Claims

What is claimed is:

1. Circuitry for preserving a logic state, comprising:

first circuitry for:

in response to a first transition of a clock signal, receiving an information signal having a logic state; and

in response to a second transition of the clock signal, latching a logic state of a first signal that indicates the received information signal's logic state;

second circuitry coupled to the first circuitry for:

in response to the second transition of the clock signal, receiving the first signal from the first circuitry; and

in response to a third transition of the clock signal, latching a logic state of a second signal that indicates the received first signal's logic state; and

third circuitry coupled to the first and second circuitry for:

during a first mode of operation, supplying power to the first and second circuitry; and

during a second mode of operation, reducing power to the first circuitry, while supplying power to the second circuitry, so that the first signal's logic state is lost, while the second signal's logic state is preserved.

2. The circuitry of Claim 1, wherein the first circuitry is coupled to a power supply during the first mode, and is decoupled from the power supply during the second mode.

3. The circuitry of Claim 2, wherein the second circuitry is coupled to the power supply during the first and second modes.

4. The circuitry of Claim 1, wherein the first transition has a first direction, the second transition has a second direction opposite from the first direction, and the third transition has the first direction.

5. The circuitry of Claim 1, wherein the first transition occurs at a start of a particular cycle of the clock signal, and wherein the third transition occurs at an end of the particular cycle.

6. The circuitry of Claim 5, wherein the second transition is between the first and third transitions.

7. The circuitry of Claim 1, wherein fourth circuitry includes the first and second circuitry, and comprising fifth circuitry coupled to the third circuitry for:

determining whether the fourth circuitry is active, and outputting an activity signal in response thereto, wherein the third circuitry is for selecting between the first and second modes in response to the activity signal.

8. The circuitry of Claim 7, wherein the third circuitry is for:

selecting the first mode during a period in response to the activity signal indicating that the fourth circuitry is active during the period; and

selecting the second mode during the period in response to the activity signal indicating that the fourth circuitry is inactive during the period.

9. The circuitry of Claim 7, wherein the fourth circuitry includes the fifth circuitry.

10. The circuitry of Claim 1, wherein the first circuitry is responsive to the first and second transitions by being edge-sensitive.

11. The circuitry of Claim 10, wherein the second circuitry is responsive to the second and third transitions by being edge-sensitive.

12. The circuitry of Claim 1, wherein the first circuitry is responsive to the first and second transitions by being level-sensitive.

13. The circuitry of Claim 12, wherein the second circuitry is responsive to the second and third transitions by being level-sensitive.

14. A method of preserving a logic state, comprising:

in response to a first transition of a clock signal, receiving an information signal having a logic state;

in response to a second transition of the clock signal, latching with first circuitry a logic state of a first signal that indicates the information signal's logic state;

in response to a third transition of the clock signal, latching with second circuitry a logic state of a second signal that indicates the first signal's logic state; and

during a first mode of operation, supplying power to the first and second circuitry; and

during a second mode of operation, reducing power to the first circuitry, while supplying power to the second circuitry, so that the first signal's logic state is lost, while the second signal's logic state is preserved.

15. The method of Claim 14, wherein supplying power to the first circuitry comprises coupling the first circuitry to a power supply during the first mode, and wherein reducing power to the first circuitry comprises decoupling the first circuitry from the power supply during the second mode.

16. The method of Claim 15, wherein supplying power to the second circuitry comprises coupling the second circuitry to the power supply during the first and second modes.

17. The method of Claim 14, wherein the first transition has a first direction, the second transition has a second direction opposite from the first direction, and the third transition has the first direction.

18. The method of Claim 14, wherein the first transition occurs at a start of a particular cycle of the clock signal, and wherein the third transition occurs at an end of the particular cycle.

19. The method of Claim 18, wherein the second transition is between the first and third transitions.

20. The circuitry of Claim 14, wherein fourth circuitry includes the first and second circuitry, and comprising:

determining whether the fourth circuitry is active, and outputting an activity signal in response thereto; and

selecting between the first and second modes in response to the activity signal.

21. The circuitry of Claim 20, wherein selecting comprises:

selecting the first mode during a period in response to the activity signal indicating that the fourth circuitry is active during the period; and

selecting the second mode during the period in response to the activity signal indicating that the fourth circuitry is inactive during the period.

22. The method of Claim 14, wherein latching with the first circuitry comprises latching with the first circuitry in response to the second transition by being edge-sensitive.

23. The method of Claim 22, wherein latching with the second circuitry comprises latching with the second circuitry in response to the third transition by being edge-sensitive.

24. The method of Claim 14, wherein latching with the first circuitry comprises latching with the first circuitry in response to the second transition by being level-sensitive.

25. The method of Claim 24, wherein latching with the second circuitry comprises latching with the second circuitry in response to the third transition by being level-sensitive.